What is claimed is:

1. A microelectronic die comprising:

first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential signal within the microelectronic die, said first and second differential signal lines being substantially parallel to one another;

wherein each of said first and second differential signal lines provides a return path for a signal on the other of said first and second differential signal lines, said return path being the predominant return path for each respective signal.

2. The microelectronic die of claim 1, comprising:

at least one trace on a second metal layer of the microelectronic die, said at least one trace being capacitively coupled to and non-parallel with said first and second differential signal lines.

3. The microelectronic die of claim 2, wherein:

said at least one trace is substantially orthogonal to said first and second differential signal lines.

4. The microelectronic die of claim 2, wherein:

said at least one trace includes a data line.

5. The microelectronic die of claim 2, wherein:

said at least one trace includes a power line.

6. The microelectronic die of claim 2, wherein:

said second metal layer is adjacent to said first metal layer.

7. The microelectronic die of claim 2, wherein:

said at least one trace includes multiple traces that are substantially parallel to one another.

8. The microelectronic die of claim 2, wherein:

said at least one trace provides a return path for a signal on said first differential signal line that has a significantly higher impedance than a return path provided by said second differential signal line.

9. The microelectronic die of claim 1, wherein:

said first and second differential signal lines are part of a clock distribution network to distribute a clock signal within the microelectronic die.

10. The microelectronic die of claim 9, wherein:

said clock distribution network uses salphasic clocking techniques to distribute said clock signal.

11. The microelectronic die of claim 9, wherein:

said clock distribution network includes a clock grid to generate, using said clock signal, a standing wave pattern for use in performing salphasic clocking, said first and second differential signal lines being part of said clock grid.

12. The microelectronic die of claim 1, wherein:

said first and second differential signal lines provide a point to point signal connection within said microelectronic die.

13. A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute said clock signal to multiple clocked elements within said microelectronic die using salphasic clocking techniques, said clock signal distribution network including at least one on-die interconnect section comprising first and second differential signal lines on a first metal layer of said

microelectronic die to carry a differential version of said clock signal, said first and second differential signal lines being substantially parallel to one another.

14. The microelectronic die of claim 13, comprising:

at least one trace on a second metal layer of said microelectronic die, said at least one trace being capacitively coupled to and non-parallel with said first and second differential signal lines.

15. The microelectronic die of claim 14, wherein:

said at least one trace is substantially orthogonal to said first and second differential signal lines.

16. The microelectronic die of claim 13, wherein:

said clock signal is sinusoidal.

17. The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of a clock grid within said clock distribution network.

18. The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of an H-tree within said clock distribution network.

19. A microelectronic die comprising:

a differential transmission line having first and second differential signal lines on a first metal layer of the microelectronic die, said first and second differential signal lines being substantially parallel to one another; and

a differential driver coupled to said differential transmission line to impart a differential signal to said differential transmission line.

20. The microelectronic die of claim 19, wherein:

each of said first and second differential signal lines provides a return path for a signal on the other of said first and second differential signal lines, said return path being the predominant return path for each respective signal.

21. The microelectronic die of claim 19, comprising:

at least one trace on a metal layer of said microelectronic die that is adjacent to said first metal layer, said at least one trace being capacitively coupled to and orthogonal to said first and second differential signal lines.

22. The microelectronic die of claim 19, comprising:

a differential receiver coupled to said differential transmission line to receive said differential signal from said differential transmission line.

23. The microelectronic die of claim 19, wherein:

said microelectronic die includes microprocessor circuitry.

24. The microelectronic die of claim 19, wherein:

said differential driver includes a buffer having a small signal differential output.

25. The microelectronic die of claim 19, wherein:

said differential transmission line is part of an on-die salphasic clock distribution network.